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MODULAR MFP/PRINTER ARCHITECTURES

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TECHNICAL FIELD

The present invention relates to the intra-system architecture of peripheral devices and multifunction peripheral devices and, more particularly, to the modularization of such architecture to take advantage of packet-switched interconnect technology.

BACKGROUND

The intra-system architectures of peripheral devices such as printers, scanners, copiers, and fax machines, or multifunction peripheral (MFP) devices which combine two or more peripheral devices into a single device, have conventionally been designed with an emphasis toward the integration of functions or systems. Thus, an MFP device having both printing and scanning capabilities typically includes as part of its intra-system architecture, an application specific integrated circuit (ASIC) which is designed to perform the functions of both the printer system and the scanner system. In addition to the printer and scanner systems, other systems such as the input-output (IO) system and a processor core may also be integrated into the single ASIC chip.

Several factors have traditionally encouraged the use of highly integrated ASICs in MFP and printer architectures. One such factor is cost. By integrating many systems or circuits onto a single ASIC chip, various pins are shared among systems which reduces the overall pin-count required to implement all of the systems, thereby reducing the cost. Furthermore, as higher volumes of a particular ASIC are produced and used in a product, the cost for each ASIC drops, thereby reducing the overall product cost.

Another factor that has encouraged the use of more highly integrated ASICs in MFP and printer architectures is interconnect technology performance. The chip-to-chip and backplane interconnect technology traditionally used in MFP and printer architectures has been the PCI (peripheral component interface) bus. PCI bus architectures typically

have a hierarchy of shared multi-drop buses which rely on address broadcasting to alert target systems of a transaction, thus limiting communications over the bus to one system at a time. System components are plugged into the bus according to their required performance levels, with low performance systems being plugged into lower performance buses that are bridged to higher performance buses so as to not burden higher performance systems.

Shared multi-drop buses have recently begun to reach their full performance potential, and techniques such as increasing bus frequency and widening the bus interface have been applied to gain higher levels of bus throughput. As bus frequency and width increase however, the ability to have more than a few systems attached to a shared bus becomes a difficult design challenge due to the corresponding need to reduce the number of electrical loads (e.g., systems) on a single bus. This challenge has in turn encouraged a higher level of system integration onto ASIC chips. Therefore, both product cost and the state of system interconnect technology have tended to support the use of more highly integrated ASICs in MFP and printer architectures.

Unfortunately, there can be significant disadvantages to using more highly integrated ASICs in the design of printer and MFP devices. Generally, ASICs that are highly integrated require higher development costs when they are newly designed or redesigned, are not leveragable across products, and increase the time to market for new products. These disadvantages are more pronounced in a market environment increasingly driven by rapid technological innovation. Time to market for a new peripheral device is key to its success, and rapid technological innovation drives the need to quickly release new products to the market in order to capture the benefits of new technology. In such an environment, highly integrated ASICs, limited to use in specific peripheral products, create a significant bottleneck in the development of newly designed peripheral devices.

For example, an MFP device having printer and scanner functions may be redesigned to integrate a fax function as well. This change would seemingly only require the effort of integrating a fax system onto a prior ASIC which already includes a printer and scanner system. However, each time an ASIC is redesigned to alter one of its integrated systems or to add a new system, every system on the ASIC must be reverified to ensure that a bug or architectural flaw has not been introduced in the process. This process is costly, since ASIC development involves the separate work of hardware and software engineers, with the software engineers having to wait for the first silicon to become available from an ASIC design before implementing code to test and verify the different systems integrated onto the ASIC. Therefore, the need to quickly turn new technology into a peripheral product and release it to market is very difficult to meet when highly integrated ASICs, limited to use in specific peripheral products, are being used in new peripheral product designs.

Finally, the use of highly integrated ASICs in intra-system architectures does not exploit the potential advantages that immerging packet-switched interconnect technologies can provide. In general, systems in peripheral devices such as printers, scanners, and fax machines are increasingly required to handle higher volumes of information as colors are used, resolutions are increased, more electronic equipment is digitalized, and general networking environments progress. For example, a printer was once the output device connected to a host computer. Today, a printer can directly output data from a scanner and digital camera without using a host computer.

Therefore, to support the higher performance demands of peripheral devices, system interconnect buses must carry much higher volumes of information. However, conventional shared multi-drop PCI bus technologies have begun to reach their full potential over the past number of years, as mentioned above, and new, high performance packet-switched interconnect technology is available. Packet-switched interconnect technology allows point-to-point, moderately parallel interconnects through a switch

fabric that permits a flattened (rather than hierarchical) architecture that uses fewer interface pins while providing greater transmission distance, lower transaction latency, and higher bandwidth.

Thus, where performance limited PCI hierarchical shared bus architectures benefit from the use of highly integrated ASICs, the enhanced performance and reduced pin count per interface available with packet-switched interconnect technology diminishes the need for highly integrated system architectures.

SUMMARY

Modularized intra-system architectures for printer and multifunction peripheral (MFP) devices are based on disintegrating traditionally highly integrated systems into separate system components which incorporate immerging packet-switched interconnect technologies. Where the performance levels of conventional shared multi-drop bus architectures using more highly integrated systems have peaked, the modularized MFP/printer architectures utilizing packet-switched interconnect technology significantly increase the performance of peripheral devices while providing the benefits of reduced costs and quicker time to market for newly designed peripheral products.

In a specific implementation, an MFP device has an internal modular architecture which includes each of the main systems integrated onto separate ASIC (application specific integrated circuit) chips. Thus, a printer system, a scanner system, an input/output (IO) system, and a processor are each integrated onto separate ASIC chips. The systems are interconnected through a switch fabric which routes packet-based data between the systems based on destination addresses embedded in the packets. The packet-based data is routed between the switch fabric and each of the systems through switch IO buses which provide a dedicated, point-to-point connection between the switch fabric and each system.

In another implementation, the intra-system architecture of a printer device is similarly modularized to include its main functional systems each integrated onto separate ASIC chips. The printer system, an IO system, and a processor system are each integrated onto separate ASIC chips. The systems are coupled to one another through a switch fabric which routes packet-based data between the systems through switch IO buses as described above.

An example of a packet-switched interconnect technology suitable for use with the modularized MFP/printer architectures described herein is the open standard RapidIO™. RapidIO™ is being developed and promoted as an open standard by the RapidIO™ Trade Association. Other packet-switched interconnect technologies may also be suitable, such as the proprietary standard, Lightning Data Transport (LDT) being developed by Advanced Micro Devices.

The modular MFP/printer intra-system architectures using packet-switched interconnect technology are capable of data transfer rates in the gigabyte per second range. This is a significant performance advantage over prior MFP/printer architectures using conventional shared multi-drop buses, such as PCI (peripheral component interface), which have data transfer rates limited to a few megabytes per second. The modularized packet-switched architectures have lower transaction latency, higher bandwidth, and fewer pins per system than is possible using a shared bus architecture. Peripheral system functions in MFP and single peripheral/printer devices are implemented through separate ASIC systems which communicate through packet-based transactions and are connected through packet-switched interconnects that provide dedicated, point-to-point, and moderately parallel data paths.

Implementing peripheral functions through individual system ASICs has additional advantages in the production of MFP, peripheral, and printer devices. For example, the individual system ASICs are available for use across multiple product lines, rather than being limited to use in a specific peripheral product as is the case with highly integrated

ASIC systems. In addition, minor design changes need only affect specific systems rather than requiring the redevelopment and reverification of an entire highly integrated ASIC.

BRIEF DESCRIPTION OF THE DRAWINGS

The same reference numbers are used throughout the drawings to reference like components and features.

Fig. 1 illustrates a workstation and a peripheral device as a suitable system environment in which to implement modular MFP and peripheral/printer architectures.

Fig. 2 is a block diagram illustrating a system such as that in **Fig. 1**.

Fig. 3A illustrates a modular intra-system architecture for an MFP device.

Fig. 3B is a flow diagram illustrating an example transaction within the modular intra-system architecture for the MFP device of **Fig. 3A**.

Fig. 4 illustrates a further modularization of the intra-system architecture within the MFP device of **Fig. 3**.

Fig. 5 illustrates a modular intra-system architecture for an MFP device similar to that shown in **Fig. 3** including switch IO bus interconnects directly coupling ASIC systems.

Fig. 6 illustrates a modular intra-system architecture for an MFP device similar to that shown in **Fig. 4** where a bridge has been replaced with a second switch IO fabric.

Fig. 7 illustrates a modular intra-system architecture for a single printer device.

Fig. 8 illustrates a modular intra-system architecture for a single printer device having multiple processors.

Fig. 9 illustrates a modular intra-system architecture for an inkjet printer having no processors.

DETAILED DESCRIPTION

The modular MFP (multifunction peripheral) and printer architectures described herein relate to intra-system interconnections between integrated circuit chips, such as ASICs (application specific integrated circuits), and the PCBs (printed circuit boards) which these chips populate. The modular architectures utilize packet-switched interconnect technology to achieve chip to chip and board to board data transfer rates in the gigabyte per second range. In addition to improving the performance of new and existing MFP and printer platforms, the partitioning of functions intrinsic to the modularized architectures permits the application of functional systems across numerous product lines, which in turn results in reduced costs for MFP and printer products.

Part of the cost reduction relates to the economies of scale which result from being able to use modular ASIC systems in numerous products, as opposed to relying on highly integrated ASIC systems which are confined to use in a single product. Additional benefits include reduced engineering costs and faster time to market for newly designed MFP and printer products. Developing and testing a single system on a modularized ASIC for a new product design, as opposed to redeveloping and retesting every system on a highly integrated ASIC, requires fewer engineering resources and allows new MFP and printer technology to hit the market faster.

Exemplary Environment for Modular Architectures

Fig. 1 illustrates an example of an environment which is suitable for implementing modular MFP and printer architectures as described herein. The system **100** of **Fig. 1** includes a peripheral device **102** connected to a host computer **104** through a direct or network connection **106**. Network connections **106** can include LANs (local access networks), WANs (wide area networks), or any other suitable communication link. The peripheral device **102** may be a printer, a scanner, a copier, a fax machine, or other such device, or may also be a multifunction peripheral (MFP) device which combines the functionality of two or more peripheral devices into a single device.

The host computer **104** outputs host data to the peripheral device **102** in a driver format suitable for the device **102**, such as PCL or postscript for a printer device **102**. The peripheral device **102** converts the host data and outputs it onto an appropriate recording media.

Fig. 2 illustrates an example of system **100** in more detail. The peripheral device **102** has a formatter/controller **200** that processes the host data. The formatter/controller **200** typically includes a data processing unit or CPU **202**, a volatile memory **204** (i.e., RAM), and a non-volatile memory **206** (e.g., ROM, Flash). The example peripheral device **102** of **Fig. 2** is an MFP device including both a printer system **208** and a scanner system **210**. In general however, the peripheral device **102** may include just a single system such as the printer system **208**, or may include systems in addition to the printer system **208** and scanner system **210**. Each system is preferably implemented as a distinct ASIC which communicates through the switch IO fabric **212**, as discussed below with reference to subsequent **Figs. 3-9**. In the configuration of **Fig. 2**, the printer system **208** and scanner system **210** use the same formatter/controller **200** which processes the host data as appropriate for output to the print engine **214**, or, it processes the data from the scanner **216** for output back to the print engine **214** as when making a copy, or back to the host **104** when scanning back to the host.

The host computer **104** includes a processor **218**, a volatile memory **220** (i.e., RAM), and a non-volatile memory **222** (e.g., ROM, hard disk, floppy disk, CD-ROM, etc.). The host computer **104** may be implemented, for example, as a general-purpose computer, such as a desktop personal computer, a laptop, a server, and the like. The host computer **104** implements one or more software-based peripheral drivers **224** that are stored in non-volatile memory **222** and executed on the processor **218**. The peripheral driver(s) **224** configure data into an appropriate format (e.g., PCL, postscript, etc.) and output the formatted data to the peripheral device **102**.

Exemplary Packet-Switched Interconnect Technology

Various packet-switched interconnect technologies that are now available or currently being developed, such as RapidIO™ and Lightning Data Transport (LDT), may be suitable for use with the modular intra-system architectures described throughout this disclosure. LDT is a proprietary standard being developed by Advanced Micro Devices. RapidIO™ is an open standard being developed and promoted by the RapidIO™ Trade Association. Although RapidIO™ is referenced throughout this disclosure in portraying the modular intra-system architectures, other similar interconnect technologies may be appropriately used.

RapidIO™ is a low pin count, packet-switched, intra-system interconnect that furnishes a switch fabric to attach a distributed network protocol management subsystem. In general, switch fabric or switch IO fabric, as used throughout this disclosure in the summary, detailed description, and claims, is an interconnect that includes a processor, memory, and memory mapped IO interface optimized for use inside a chassis. The processor circuitry and its programming control the switching paths of the fabric. Data transactions between systems coupled to the switch fabric are based on packets, with each packet having a source specified destination address which instructs the switch fabric where the packet is to be routed. This method of source routing burdens only the path between the sending and receiving system with each transaction, leaving open bandwidth on other paths and enabling concurrent communications between additional systems.

Control symbols within packets manage the flow of transactions through the switch fabric and between the various systems. Control symbols are used for packet acknowledgement, flow control information, and maintenance functions. Maintenance functions involve tasks such as error detection and recovery. Flow control permits various systems to communicate through the switch fabric concurrently, rather than systems having to take turns communicating over a bus as occurs with traditional shared multi-drop bus architectures.

RapidIO™ is specified in a 3-layer hierarchy of logical, transport, and physical specifications. The logical specification defines the overall protocol and packet formats necessary for endpoint systems to process a data transaction. The transport specification provides the necessary route information for a packet to move from one system to another. The physical specification contains the system level interface such as packet transport mechanisms, flow control, electrical characteristics, and low level error management. RapidIO™ can be understood in greater detail with reference to the RapidIO™ specification. The RapidIO™ specification can be obtained through the RapidIO™ Trade Association and is expressly incorporated herein by reference.

Exemplary Modular MFP and Printer Architectures

Fig. 3A illustrates a modular intra-system architecture for an MFP device which has both printer and scanner capabilities. The modular architecture includes a separate ASIC chip for each of the main MFP systems. Thus, the printer system **300**, the scanner system **302**, the IO (input/output) system **304**, and the processor system **306** are each separately integrated onto distinct ASICs. Each ASIC system incorporates packet-switched technology, and the intra-system architecture includes a switch IO fabric **308** and switch IO buses **310** interconnecting each system for the purpose of transferring data. The switch IO buses **310** connecting each system to the switch IO fabric **308** provide dedicated (i.e., non-shared), point-to-point interconnects.

Although the MFP device of **Fig. 3A** includes only printer and scanner functions, additional peripheral functions can also be included, such as facsimile and copy functions. The modular intra-system architecture permits the addition of functions by interconnecting their respective systems to the switch IO fabric **308** through additional dedicated switch IO buses **310**. In addition, multi-processor systems can be easily configured by interconnecting additional processors to the switch IO fabric **308** through switch IO buses **310**. A multi-processor system is illustrated in **Fig. 8**.

Each system in the MFP architecture of **Fig. 3A** is a separate module designed to perform its specific system functions and to interact within the modularized intra-system architecture using packet-switched interconnect technology. Therefore, inherent to the design of each modular ASIC system, is the packet-switched interconnect technology being used in the intra-system architecture, such as RapidIO™. Thus, in addition to performing typical functions such as pipelining images and controlling the print engine, the printer system **300** is designed to operate within the modularized architecture where data transactions are based on the RapidIO™ packet-switched technology. Details of the RapidIO™ packet-switched technology which are necessarily integrated into each modular ASIC system can be found in the RapidIO™ specification, incorporated by reference above.

An example transaction within the MFP architecture of **Fig. 3A** is illustrated by the flow diagram of **Fig. 3B**. An initiating system, such as the processor system **306**, generates a request packet at operation **320**, which is transmitted to a target system, such as the printer system **300**. First, the packet is sent from the processor system **306** to the switch IO fabric **308** at operation **322**, through the dedicated switch IO bus **310(1)**. The switch IO fabric **308** replies with an acknowledge control symbol at operation **324**, which it sends back to the processor system **306** through switch IO bus **310(1)**. The switch IO fabric **308** also forwards the request packet on to the target printer system **300** through switch IO bus **310(2)**. The printer system **300** completes the transaction and generates a response packet at operation **326**. The response packet is then sent through the switch IO bus **310(2)** to the switch IO fabric **308** at operation **328**, and on to the processor system **306** through switch IO bus **310(1)** at operation **330**, using control symbols to acknowledge each transfer. When the response packet reaches the initiating processor system **306** and is acknowledged at operation **332**, the transaction is complete.

While such transactions take place between the processor **306** and printer **300** systems, additional transactions may occur simultaneously between other systems. For

example, while the transaction between the processor system **306** and the printer system **300** is taking place, a similar transaction may be taking place between the scanner system **302** and the IO system **304**. In general, data transactions occur in a similar fashion within each of the subsequently described modular architectures of **Figs. 4-9**.

Although various advantages of the modularized architectures have been briefly mentioned, having introduced an exemplary intra-system architecture in **Fig. 3A**, particular advantages associated with the use of modular ASIC systems as opposed to highly integrated ASIC systems are more readily apparent. For example, a minor advance in print engine technology may cause a change in the print engine **312** of **Fig. 3A**. This change may alter the interface **314** to the print engine **312** which in turn requires a minor redesign of the printer system **300**. In a traditional PCI bus architecture where a highly integrated ASIC might include all the main peripheral systems (i.e., the printer system **300**, the scanner system **302**, the IO system **304**, and the processor system **306**), a minor redesign of the printer system **300** would require redeveloping and reverifying each system on the ASIC. In the modularized architecture illustrated in **Fig. 3A**, however, the minor redesign of the printer system **300** only requires redeveloping and reverifying the single printer system **300** ASIC. Thus, the length of development cycles and the associated engineering costs for new products are significantly reduced.

Fig. 4 illustrates a further modularization of the intra-system architecture within the MFP device represented by **Fig. 3A**. In **Fig. 4**, the IO system ASIC **304** has been separated from the PCI bus **316**. The PCI bus **316** connects EIO (enhanced input/output) ports **318** to the intra-system architectures in both **Figs. 3A** and **4**. Generally, EIO ports **318** permit additional IO devices, such as hard drives, network cards, or other third party functions, to be connected to printers and other peripheral devices. In **Fig. 3A**, the PCI bus **316** and EIO ports **318** are connected to the intra-system architecture through the IO system ASIC **304**, while in **Fig. 4** they are connected through a bridge **400**. The bridge **400** connects the PCI bus **316** and EIO ports **318** directly to the switch IO fabric **308**

through an additional switch IO bus **310(5)**. The bridge **400** essentially permits data transactions to move between the packet-based architecture and the PCI bus architecture.

The benefit of the further modularization demonstrated by the architecture of **Fig. 4** is similar to that discussed above with respect to the architecture of **Fig. 3A**. That is, the further modularization of the IO system ASIC **304** illustrated in **Fig. 4** provides the added benefit of not having to reverify the PCI block **316** in the event that the IO system ASIC **304** is changed. For example, if a new IO standard is adopted, new printer/peripheral designs would be necessary to enable connection using the new standard. Such a change would require a change to the IO system ASIC **304**. Under these circumstances, the architecture of **Fig. 3A** requires that the IO system ASIC **304** along with the entire PCI block **316** be reverified. By contrast, the further modularized architecture of **Fig. 4** avoids the reverification of the PCI block **316**, because it is no longer affected by changes to the IO system ASIC **304**.

Fig. 5 illustrates a modular intra-system architecture for an MFP device similar to that shown in **Fig. 3A**. However, the architecture of **Fig. 5** includes additional high speed, switch IO bus **310** interconnects placed directly between ASIC systems. Specifically, a dedicated point-to-point switch IO bus **310(6)** couples the printer system ASIC **300** directly to the IO system ASIC **304**, and another switch IO bus **310(7)** couples the printer system ASIC **300** directly to the scanner system ASIC **302**.

These additional bus interconnects are possible because of the reduced number of pins generally required to implement the modular architectures illustrated in **Figs. 3A** and **5**. Since the interface between a switch IO bus **310** and a modular system ASIC requires significantly fewer pins than are necessary for similar interfaces in a traditional PCI bus architecture, there are free pins available on the modular system ASICs which can be used for additional bus interfaces.

The additional switch IO bus **310(6-7)** interconnects between systems illustrated in the modular architecture of **Fig. 5** offer added performance benefits over the modular

architecture of **Fig. 3A**. Although the switch IO fabric **308** provides data throughput rates significantly greater than traditional shared multi-drop PCI bus architectures, there is some transaction latency introduced by the switch IO fabric **308**. Thus, where the switch IO fabric **308** can be avoided in data transactions, performance is further improved by eliminating the delay introduced going back and forth through the switch IO fabric **308**.

The architecture of **Fig. 5** therefore illustrates a direct, high speed, switch IO bus **310(6)** interconnect between the printer system ASIC **300** and the IO system ASIC **304** which improves communication between these systems and is available by virtue of the reduction in pin count achieved through a modularized intra-system architecture. A similar switch IO bus **310(7)** interconnect is shown between the printer system ASIC **300** and the scanner system ASIC **302**. Additionally, the architecture illustrated in **Fig. 5** is not meant to limit the number or configuration of these system to system interconnects. That is, such direct interconnects can exist between other systems wherever pin space is available and data transactions are appropriate.

Fig. 6 illustrates a modular intra-system architecture for an MFP device similar to that shown in **Fig. 4**. However, in the modular architecture of **Fig. 6**, the PCI bus **316** has been eliminated, and the switch IO to PCI bridge **400** has been replaced with a second switch IO fabric **600**. In addition, EIO devices **602** are plugged into connectors **604** that are coupled to the second switch IO fabric **600** through additional switch IO bus **310(8-10)** interconnects.

The second switch IO fabric **600** electrically isolates the EIO devices **602** from one another. Thus, the architecture in **Fig. 6** permits the installation and removal of EIO devices **602** via connectors **604** without having adverse electrical impact on the transmission of data. By contrast, the intra-system architecture shown in **Fig. 4**, which utilizes a PCI bus to interconnect with EIO ports **318**, does not provide the same electrical isolation. When EIO devices are added or removed from the EIO ports **318** of **Fig. 4**, the electrical load can change on the PCI bus **316** which may alter the amplitude of data

signals and result in incorrect data transmissions. In general, the modular architecture of **Fig. 6** illustrates the benefit of electrical isolation provided by the switch IO fabric which is important where systems or devices are installed and removed by hand.

Fig. 7, in one respect, illustrates a modular intra-system architecture for a single printer device represented on PCB **700**. The PCB **700** for the printer architecture therefore includes the printer system **300**, the IO system **304**, and the processor system **306** each separately integrated onto distinct ASICs, without any additional peripheral device system ASICs connected to the switch IO fabric **308**. The intra-system interconnects made through the switch IO fabric **308** and switch IO buses **310** are similar to those described above with respect to the various MFP device architectures.

In addition, the architecture shown on the PCB **700** of **Fig. 7** is not limited to representing a single printer device, but might also represent other singular, as opposed to multifunction, peripheral device architectures. That is, the modular intra-system architectures described herein are applicable to single peripheral devices such as printers, scanners, facsimiles, and copiers, in addition to being applicable to MFP devices which combine two or more peripheral devices.

In a second respect, **Fig. 7** illustrates that the format control of the printer platform on PCB **700** can be easily shared by other peripheral systems not resident on the same PCB **700**. This is possible because the switch-based interconnects used in the modular architecture can traverse connectors. Thus, the switch IO bus **310(11)** traverses the connector set **702**, permitting interconnection between the printer platform PCB **700** and the scanner platform PCB **704**. The connector set **702** intersection is represented by the hashed arrow **706** between PCB **700** and PCB **704**.

Fig. 8 illustrates a modular intra-system architecture for a single printer device having multiple processors **306**. The modular intra-system architecture permits the addition of processors by interconnecting them to the switch IO fabric **308** through additional switch IO buses **310(12-13)** as shown by the two processors **306** on PCB **800**

of **Fig. 8**. In addition, a processor system on a separate PCB **802** can be added to the architecture of PCB **800** through a switch IO bus **310(14)** traversing a connector set **804**. The connector set **804** intersection is represented by the hashed arrow **806** between PCB **800** and PCB **802**.

Although the modular multi-processor architecture shown in **Fig. 8** is embodied in a single printer device, it is not limited to this embodiment. That is, the modular multi-processor architecture shown in **Fig. 8** is equally applicable to other single peripheral devices such as scanners, facsimiles, and copiers, as well as MFP devices which combine two or more peripheral devices.

Fig. 9 illustrates a modular intra-system architecture for a single inkjet printer device which has no processor. Inkjet printer platforms typically do not format printer driver output, such as PCL or postscript languages. Instead, this processing is done on the host computer, which sends pre-formatted data to the inkjet printer system.

For inkjet printers, or other peripheral devices which do not require an on-board processor, the modularized printer (or peripheral) system ASIC **300** can be directly interfaced to the IO system ASIC **304**. The high speed performance benefits are therefore derived from the packet-based data transmission technology, in addition to the ability to use the printer (or peripheral) system ASIC **300** and the IO system ASIC **304** across different product lines.

Although the description above uses language that is specific to structural features and/or methodological acts, it is to be understood that the invention defined in the appended claims is not limited to the specific features or acts described. Rather, the specific features and acts are disclosed as exemplary forms of implementing the invention.